Amendments to the specification:

Please replace the fourth paragraph on page 5 with the following amended paragraph:

Loop Kb sets the Q of the filter 100. Loop Kb consists of a gain summation block 104, transfer function block 106 (S-A)/(S+A), gain summation block 112, and passband frequency tuning block 108. In a preferred embodiment of the present invention, the Q of the filter 100 could be controlled from 5 to 300. The Q of the filter 100 is preferably controlled by a Q control ~~1124~~, which is a 10- bit gain control for loop Kb.

Please replace the first full paragraph on page 6 beginning on line 6 with the following amended paragraph:

The present invention may be best implemented using the following formula: Y

$$= \left[\frac{K_3 - K_1 K_2}{1 + K_4 K_2}\right]\left[\left[\frac{S(B-A)}{S^2 + S(A+B)\left[\frac{1-K_4K_2}{1+K_4K_2}\right] + (A \bullet B)}\right] + \left[\frac{S^2 - (A \bullet B)}{S^2 + S(A+B)\left[\frac{1-K_4K_2}{1+K_4K_2}\right] + A \bullet B}\right]\right]$$

Where:

$S=j\omega$

K1 is the gain from Node A to the output of the blocks G1 and S1.

K4 is the gain from Node F to the output of the block S1, Node C.

K3 is the gain from Node D to the output of the block S1, the Output.

K2 is the gain from Node E to the output of the block S1, the Output.

In the block diagram, block S1 represents the summation of the voltages at Node A with gain K1 and Node F with the gain of K4. Block S1 represents the summation of the voltages at Node E with the gain of –K2 and Node D with the gain K3. Y1, Y2 are allpass filters, with the transfer functions of (S-A)/(S+A). Y3 is an allpass filter, with the transfer functions of (S-B)/(S+B). The value for A and B represent a value that is not dependent on the frequency. In many cases, the values for A and B will be determined by the function 1/RC, which is based upon the topology of the allpass filter. The topology of the allpass filter structure can take on many different forms to realize the same transfer function. The block S1 could also be represented as gain blocks for K1 and K4 followed by a summation network. Block S2 could also be represented as gain blocks for K3 and –1*K2 followed by a summation network. The gain and summation functions can be achieved with many different circuit topologies.